REMARKS

The Applicant thanks the Examiner and his supervisory Examiner, Matthew Smith, for the courtesy that they extended during a telephonic interview conducted on September 22, 2004 with the Applicant's attorney. As agreed during the telephonic interview, the instant response and amendment summarizes the position expressed by the Applicant during the interview.

Claims 1-23 were presented for examination. Claims 1-6 and 8-23 stand rejected. Claim 7 is objected to as being dependent upon a rejected base claim, but has been indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1-3, 17, and 23 have been amended. Applicant thanks the Examiner for examination of the claims pending in this application and addresses Examiner's comments below.

Objection to the Title

The title of the application is objected to as not being descriptive of the invention. In response, the title is amended to recite:

"Inspection of Semiconductor Devices Using Design Data."

Claim Objections

Claim 1 has been objected to because it recites "configuring of the recipe." Examiner suggested changing "configuring of the recipe" to "configuration of the recipe." In response, Applicants have amended claim 1 to recite "configuration of the recipe." Applicants respectfully request withdrawal of the objection to claim 1.

Claim Rejection Under 35 U.S.C. § 102 (e)

Claims 1-6 and 8-23 stand rejected under 35 U.S.C. § 102(e) as being unpatentable over Nara (U.S. Patent No. 6,388,747B2). Claims 1, 17, and 23 have been amended to improve readability of the claims by explicitly reciting what was previously implicit. Applicants note that these amendments do not narrow the scope of protection with respect to the prior art, or with respect to potentially infringing devices or articles. Applicants have made various other amendments to dependent claims 2 and 3 to conform the claims to their respective base claim. This rejection is respectfully traversed.

Claim 1 recites:

> For an instrument responsive to recipe parameters, a method for creating a recipe, the method comprising:
> accessing mask set data;
> recognizing a target structure in the mask set data;
> extracting parameters from the mask set data; and
> configuring the recipe based on the extracted parameters responsive to the recognized target structure, **wherein the configuration of the recipe is performed before a wafer printed with a mask created from the mask set data is generated.**

Applicant's claimed invention, as recited in claim 1, is directed to a technique that uses information from the mask data to generate a recipe for inspection/metrology systems to inspect or measure a semiconductor wafer. Claim 5 similarly recites "creating the recipe ... before a wafer ... is generated." Amended claims 17 and 23 recite a system and an instrument adapted to perform steps similar to the ones recited in claim 5. The information present in the mask data is, in many cases, sufficient to find target sites, alignment sites, and to determine the other parameters necessary to generate a recipe. An advantage of the claimed invention in that it does not require that a wafer become available for use in creating a recipe.

Nara does not disclose or suggest the claimed invention. Although Nara is directed to a system and method for setting up a recipe on an inspection tool, the configuration of the recipe is performed in a completely different manner than in the claimed invention. The inspection tools in Nara require the existence of a wafer for a given device type and layout in order to generate a recipe, thereby introducing an undesirable time lag between the time a wafer is available for a given device and a first measurement or inspection can be performed. Additionally, the method of Nara requires a skilled operator to be present to generate the recipe.

Examiner asserts in his rejection that Nara discloses "accessing mask set data" at col. 1, lines 25-30. Neither the cited passage of the reference nor the rest of the disclosure, however, disclose the claimed invention. Rather, the cited passage discloses a conventional method of manufacturing a semiconductor device by transferring a circuit pattern formed on a photomask to a semiconductor wafer by a lithographing process (Nara, col. 1, lines 25-32). The word "photomask" is used by Nara to describe conventional manufacturing process of a semiconductor device. Nara is not even concerned with accessing mask set data to generate a recipe for inspection of a semiconductor device because Nara requires existence of a wafer to generate a recipe.

Similarly, Nara does not disclose or suggest the step of "extracting parameters from the mask set data." Examiner asserts in his rejection that this step is disclosed at col. 4, lines 57-67 of Nara. Instead, the cited portions of the reference disclose:

> "...an image from an external apparatus can be displayed on the monitor of the inspection apparatus for **extracting a defect** of the inspection-subject substrate." (Emphasis added).

The cited paragraph explicitly requires the use of an image derived from observing the wafer with an imaging tool such as an optical or electron beam inspection tool. "Extracting

parameters from the mask set data," as claimed, is different from "extracting a defect of the inspection-subject substrate," as disclosed in Nara, since the mask set data from which the parameters are extracted is generated before a wafer printed with a mask created from the mask set data is generated. In contrast, in Nara, a defect is extracted from a specific wafer that is in existence when the defect is extracted.

Moreover, Nara does not disclose or suggest the recipe configuration step. Examiner cites col. 32, lines 55-65 of Nara for a disclosure of this claimed feature. The cited passage of the reference describes a diagram shown in Fig. 29 of the picture plane in the inspecting mode. As shown in Fig. 29 of Nara, region 909 displays "inspection progress" and "the number of defects." This requires the existence of a wafer. Region 908 of Fig. 29 explicitly references the location of the wafer ("Shelf Number B15) and identity code for the specific wafer ("Wafer ID22 Lot ID 11"), thereby explicitly requiring the existence of the wafer. Similarly, at col. 16, lines 19-58 Nara describes a recipe forming procedure that requires that a wafer be in existence to generate a recipe. By contrast, in the claimed invention, the configuration of the recipe is performed before a wafer printed with a mask created from the mask set data is generated.

For at least the reasons discussed above, independent claims 1, 5, 17, and 23 patentably distinguish over the cited references. Dependent claims 2-4, 6-16, and 18-22 variously depend from claims 1, 5, 17, and 23 and are patentably distinct for at least the reasons cited above in addition to reciting their own patentable features.

For example, claim 3 further recites "wherein the extracted parameters comprise at least one of wafer processing parameters, inspection parameters, and control parameters." Claim 3 is not disclosed or suggested by Nara. Col. 4, lines 30-40 of Nara cited by the Examiner to support the rejection of claim 3 disclose a user interface display in which parameters are being inputted

by a human operator of the instrument. In contrast, the parameters recited in claim 3 are extracted from the mask set data rather than being manually inputted by a human operator.

Conclusion

In sum, Applicant respectfully submits that claims 1-23, as presented herein, are patentably distinguishable over the cited reference (including references cited, but not applied). Therefore, Applicant requests reconsideration and allowance of these claims.

RESPECTFULLY SUBMITTED,
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